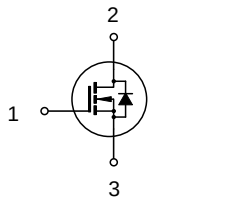
7A, 600V N-CHANNEL MOSFET

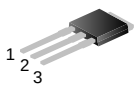
GENERAL DESCRIPTION

SVFP7N60CMJ/D is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power supplies, DC-DC converters and H-bridge PWM motor drivers.



1.Gate 2.Drain 3.Source



TO-251J-3L

TO-252-2L

FEATURES

- 7A, 600V, $R_{DS(on)(typ.)}$=0.96Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVFP7N60CMJ	TO-251J-3L	P7N60CMJ	Halogen free	Tube
SVFP7N60CDTR	TO-252-2L	P7N60CD	Halogen free	Tape&Reel

ABSOLUTE MAXIMUM RATINGS (T_A=25°C UNLESS OTHERWISE NOTED)

Characteristics		Symbol	Ratings		Unit
			SVFP7N60CMJ	SVFP7N60CD	
Drain-Source Voltage		V_{DS}	600		V
Gate-Source Voltage		V_{GS}	±30		V
Drain Current	T_C=25°C	I_D	7.0		A
	T_C=100°C		4.4		
Drain Current Pulsed		I_{DM}	28		A
Power Dissipation(T_C=25°C)		P_D	93	90	W
-Derate above 25°C			0.74	0.72	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	490		mJ
Reverse Diode dv/dt (Note 2)		dv/dt	4.5		V/ns
MOSFET dv/dt Ruggedness (Note 3)		dv/dt	50		V/ns
Operation Junction Temperature Range		T_J	-55～+150		°C
Storage Temperature Range		T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVFP7N60CMJ	SVFP7N60CD	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.34	1.39	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	62.0	°C/W

ELECTRICAL CHARACTERISTICS (T_j=25°C UNLESS OTHERWISE NOTED)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=3.5A	--	0.96	1.2	Ω
Input Capacitance	R_g	f=1.0MHz	--	5.0	--	Ω
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	770	--	pF
Output Capacitance	C_{oss}		--	96	--	
Reverse Transfer Capacitance	C_{rss}		--	8.7	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V, I_D=7.0A, R_G=25Ω (Note 4,5)	--	16	--	ns
Turn-on Rise Time	t_r		--	33	--	
Turn-off Delay Time	$t_{d(off)}$		--	52	--	
Turn-off Fall Time	t_f		--	32	--	
Total Gate Charge	Q_g	V_{DS}=480V, I_D=7.0A, V_{GS}=10V (Note 4,5)	--	21	--	nC
Gate-Source Charge	Q_{gs}		--	4.5	--	
Gate-Drain Charge	Q_{gd}		--	10	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	7.0	A
Pulsed Source Current	I_{SM}		--	--	28	
Diode Forward Voltage	V_{SD}	I_S=7.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=7.0A,V_{GS}=0V, dI_F/dt=100A/μs (Note 4)	--	482	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.9	--	μC

Notes:

1. L=30mH, I_{AS}=5.16A, V_{DD}=100V, R_G=25Ω, starting temperature T_J=25°C;
2. V_{DS}=0~400V, I_{SD}<=7A, T_J=25°C;
3. V_{DS}=0~480V;
4. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
5. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

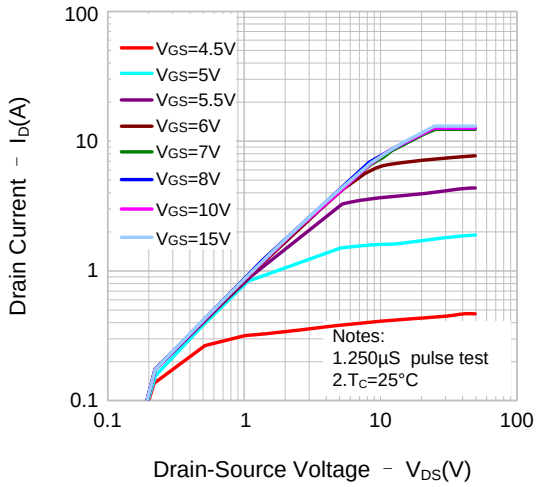


Figure 2. Transfer Characteristics

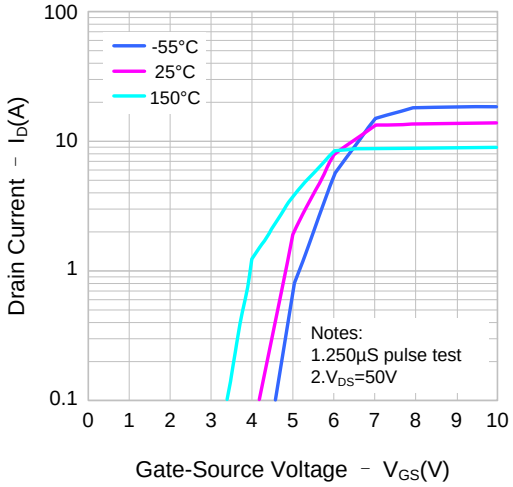


Figure 3. On-Resistance Variation vs. Drain Current

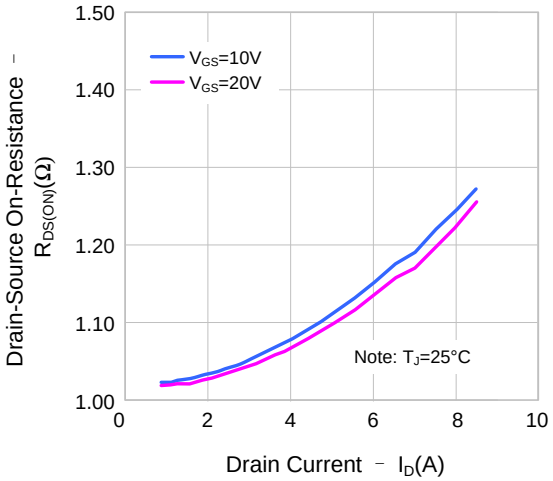


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

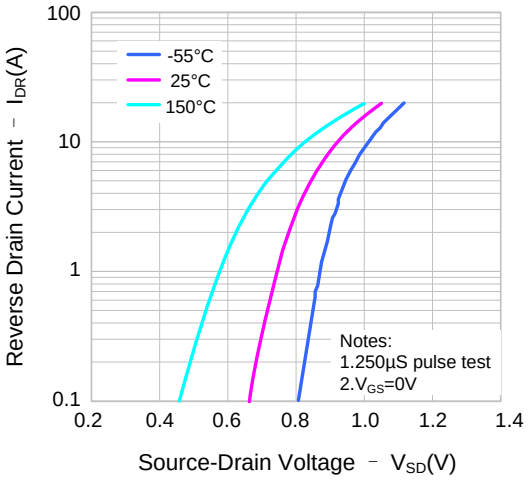


Figure 5. Capacitance Characteristics

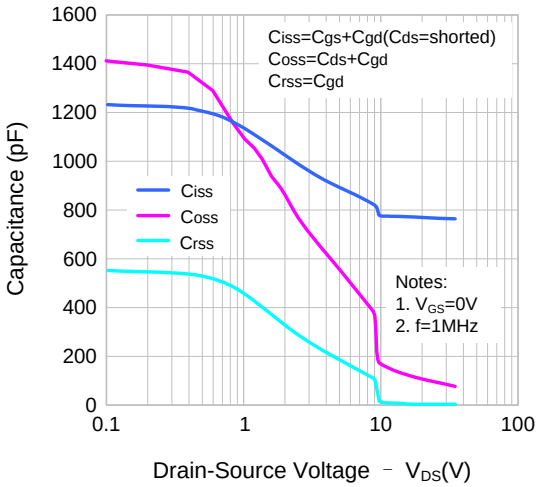
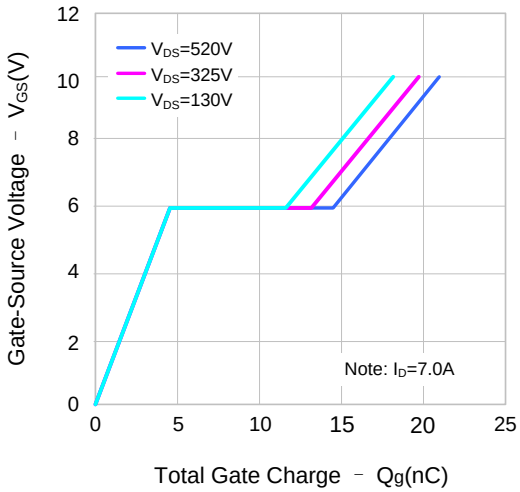


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(CONTINUED)

Figure 7. Breakdown Voltage Variation vs. Temperature

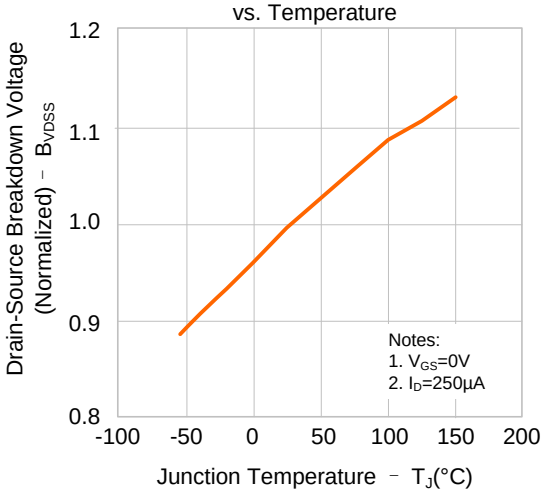


Figure 8. On-resistance vs. Temperature

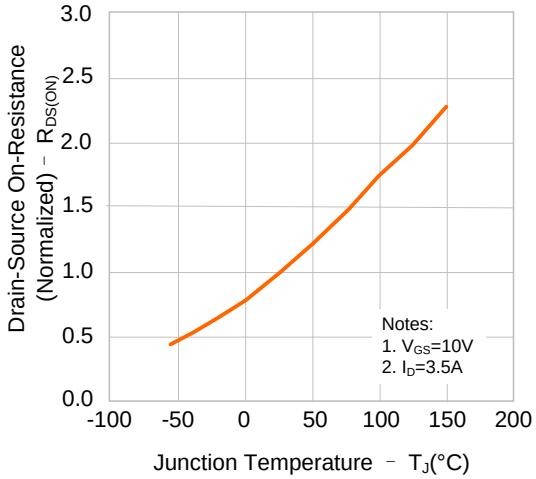


Figure 9-1. Max. Safe Operating Area (SVFP7N60CMJ)

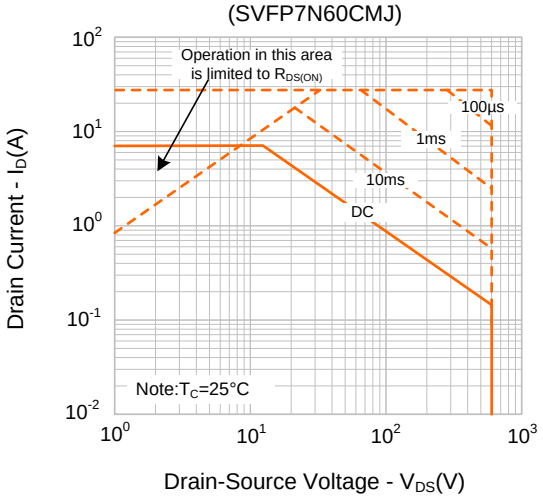


Figure 9-2. Max. Safe Operating Area (SVFP7N60CD)

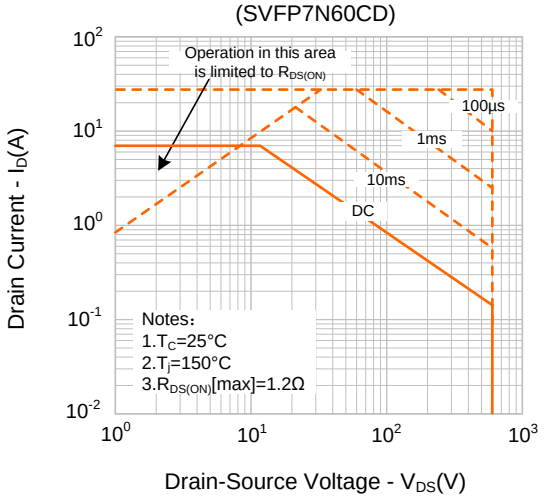
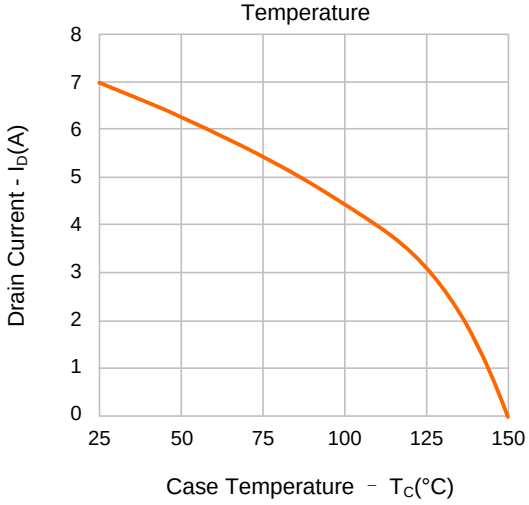
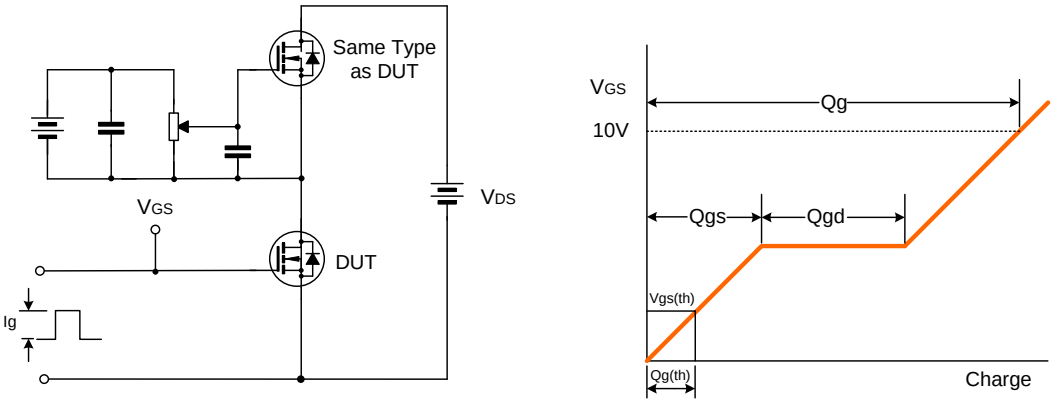


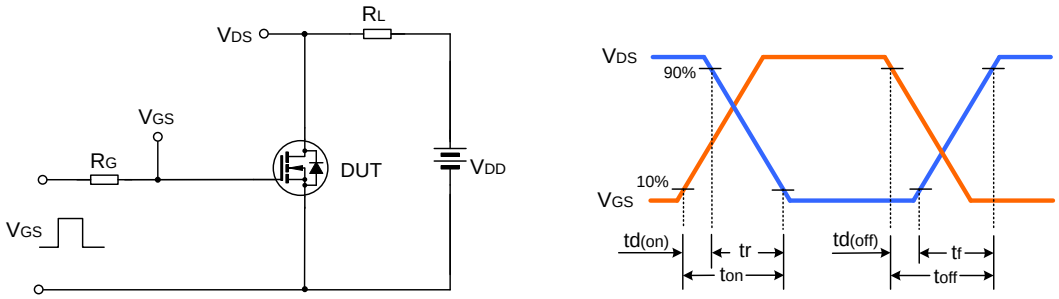
Figure 10. Max. Drain Current vs. Case Temperature



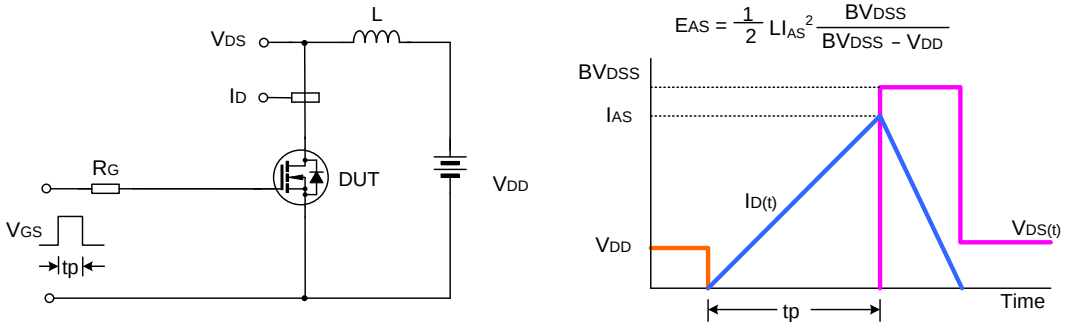
TYPICAL TEST CIRCUIT



Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

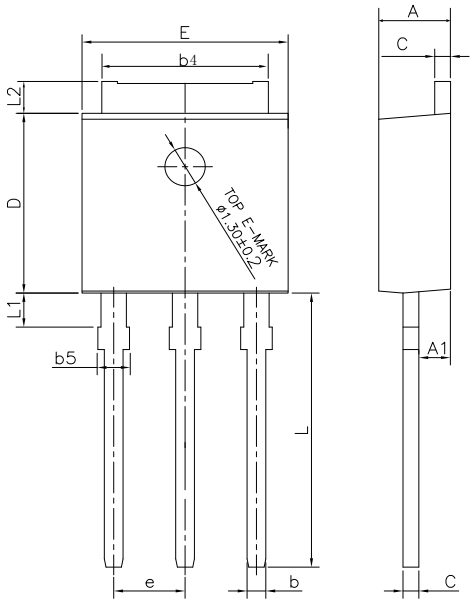


Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE OUTLINE

TO-251J-3L

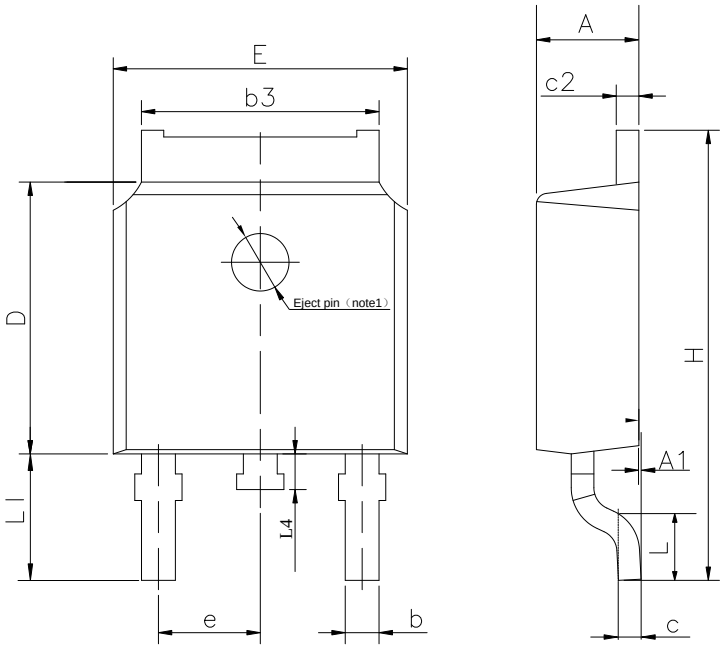
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

TO-252-2L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

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Rev.: 1.2

Revision History:

1. Modify Electrical schematic and TYPICAL TEST CIRCUIT

Rev.: 1.1

Revision History:

1. Add TO-252-2L

Rev.: 1.0

Revision History:

1. First release