

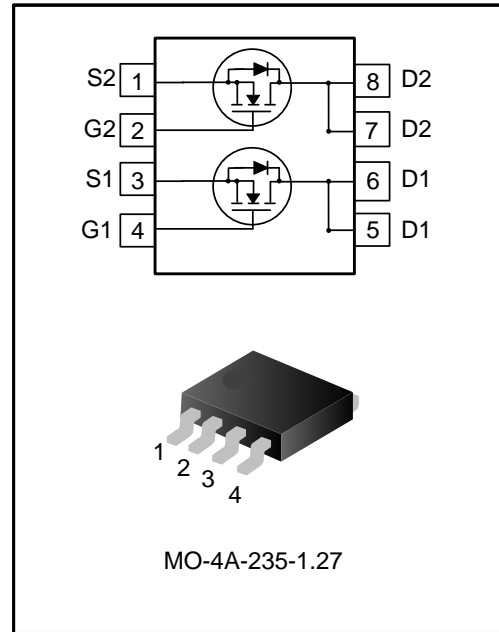
63A, 40V DUAL N-CHANNEL MOSFET

DESCRIPTION

SVGQ046R8NLPD is dual N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance and high avalanche breakdown tolerance. This device is widely used in power management for UPS and Inverter Systems.

FEATURES

- ◆ AEC-Q101 qualified
- ◆ 63A, 40V, $R_{DS(on)(typ.)}=5.6m\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Extreme dv/dt rated
- ◆ 100% avalanche tested
- ◆ Pb-free lead plating
- ◆ RoHS compliant
- ◆ Max. junction temperature: $T_{jmax.}=175\text{ }^{\circ}C$



KEY PERFORMANCE PARAMETERS

Characteristics	Ratings	Unit
V_{DS}	40	V
$V_{GS(th)}$	2.4~3.4	V
$R_{DS(on),max}$	6.8	$m\Omega$
I_D	63	A
$Q_{g,typ}$	18	nC

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SVGQ046R8NLPDTR	MO-4A-235-1.27	Q046R8NLP	Halogen free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, $T_J=25^{\circ}\text{C}$)

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Voltage	V_{DS}	--	--	--	40	V
Gate-source Voltage	V_{GS}	--	-20	--	20	V
Drain Current (Note 1)	I_D	$T_C=25^{\circ}\text{C}$	--	--	63	A
		$T_C=100^{\circ}\text{C}$	--	--	44	A
Drain Current Pulsed (Note 2)	I_{DM}	$T_C=25^{\circ}\text{C}$	--	--	252	A
Power Dissipation (Note 3)	P_D	$T_C=25^{\circ}\text{C}$	--	--	50	W
Single Pulsed Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{DD}=32\text{V}$, $R_G=25\Omega$, starting temperature $T_J=25^{\circ}\text{C}$	--	--	35	mJ
Single Pulsed Avalanche Current	I_{AS}	--	--	--	26.6	A
Operation Junction Temperature Range	T_J	--	-55	--	175	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	--	-55	--	175	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Thermal Resistance, Junction-case, Bottom	$R_{\theta JC}$	--	--	--	3.0	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-ambient	$R_{\theta JA}$	--	--	--	50	$^{\circ}\text{C}/\text{W}$
Soldering Temperature(SMD)	T_{sold}	Reflow soldering: 10 ± 1 sec, 3times	--	--	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, $T_J=25^{\circ}\text{C}$)

Static characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Drain-source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	--	--	V
Drain-source Leakage Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	--	--	1.0	μA
		$V_{DS}=40V, V_{GS}=0V, T_J=150^{\circ}\text{C}$	--	2.5	--	
Gate-source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.4	--	3.4	V
Static Drain-source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=25A$	--	5.6	6.8	$m\Omega$
Grid resistance	R_g	$f=1\text{MHz}$	--	2.3	--	Ω

Dynamic characteristics

Characteristics	Symbol	Test conditions	Ratings			Unit
			Min.	Typ.	Max.	
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=25V$	--	1053	--	pF
Output Capacitance	C_{oss}		--	357	--	
Reverse Transfer Capacitance	C_{rss}		--	28	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V, R_G=3.5\Omega, I_D=50A$ (Notes 4, 5)	--	7.3	--	ns
Turn-on Rise Time	t_r		--	25	--	
Turn-off Delay Time	$t_{d(off)}$		--	16	--	
Turn-off Fall Time	t_f		--	11	--	
Total Gate Charge	Q_g	$V_{DD}=32V, V_{GS}=10V, I_D=50A$ (Notes 4, 5)	--	18	--	nC
Gate-source Charge	Q_{gs}		--	7.4	--	
Gate-drain Charge	Q_{gd}		--	4.1	--	
Gate-plateau Voltage	$V_{plateau}$		--	6.0	--	

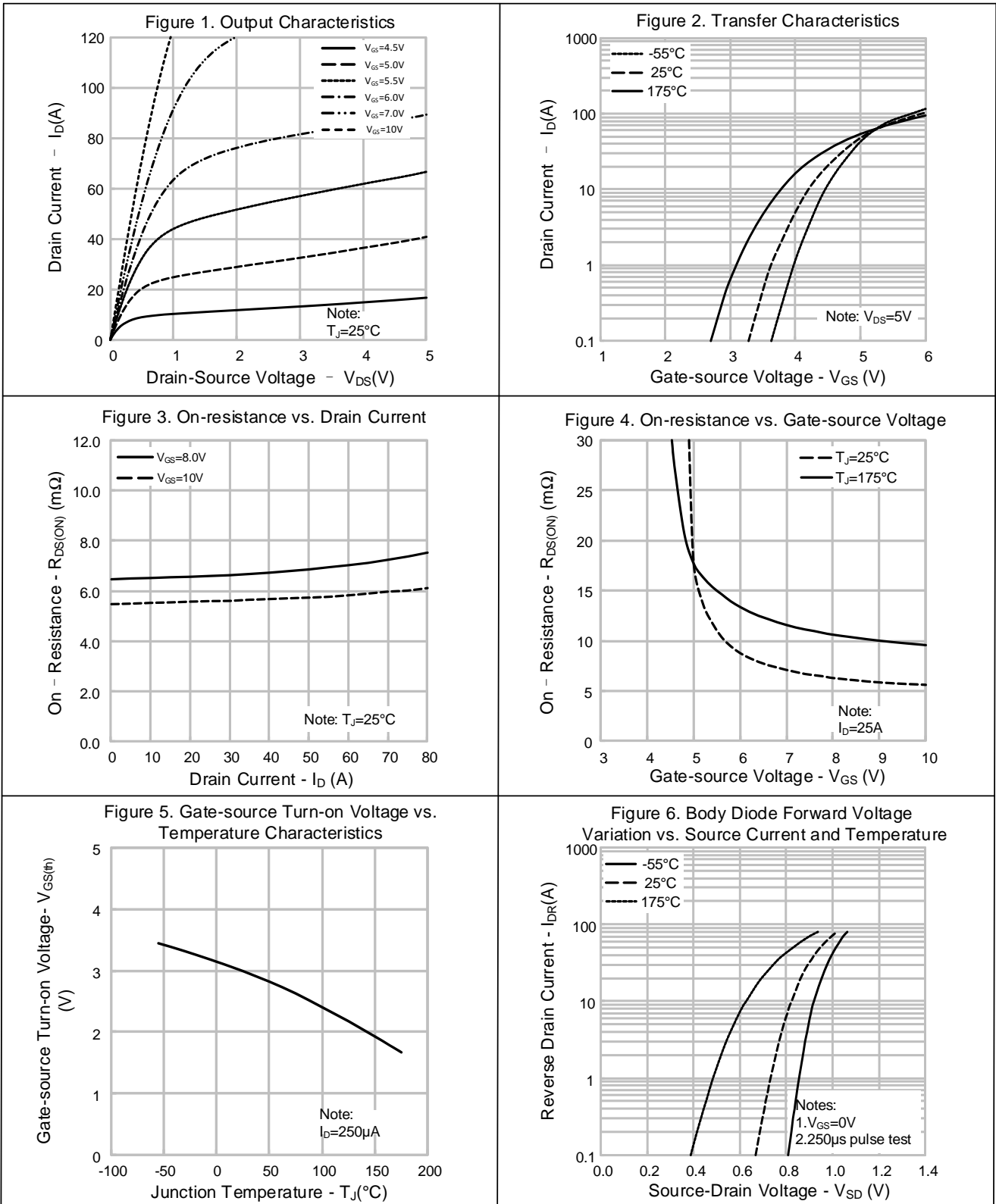
Reverse diode characteristics

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Diode Forward Current	I_S	Integral reverse P-N junction diode in the MOSFET	--	--	63	A
Diode Pulse Current	$I_{S,pulse}$		--	--	252	
Source-Drain Diode Voltage Drop	V_{SD}	$I_S=25A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=50A, V_{GS}=0V, V_R=40V, di_F/dt=100A/\mu s$ (Note 4)	--	30	--	ns
Reverse Recovery Charge	Q_{rr}		--	19	--	nC

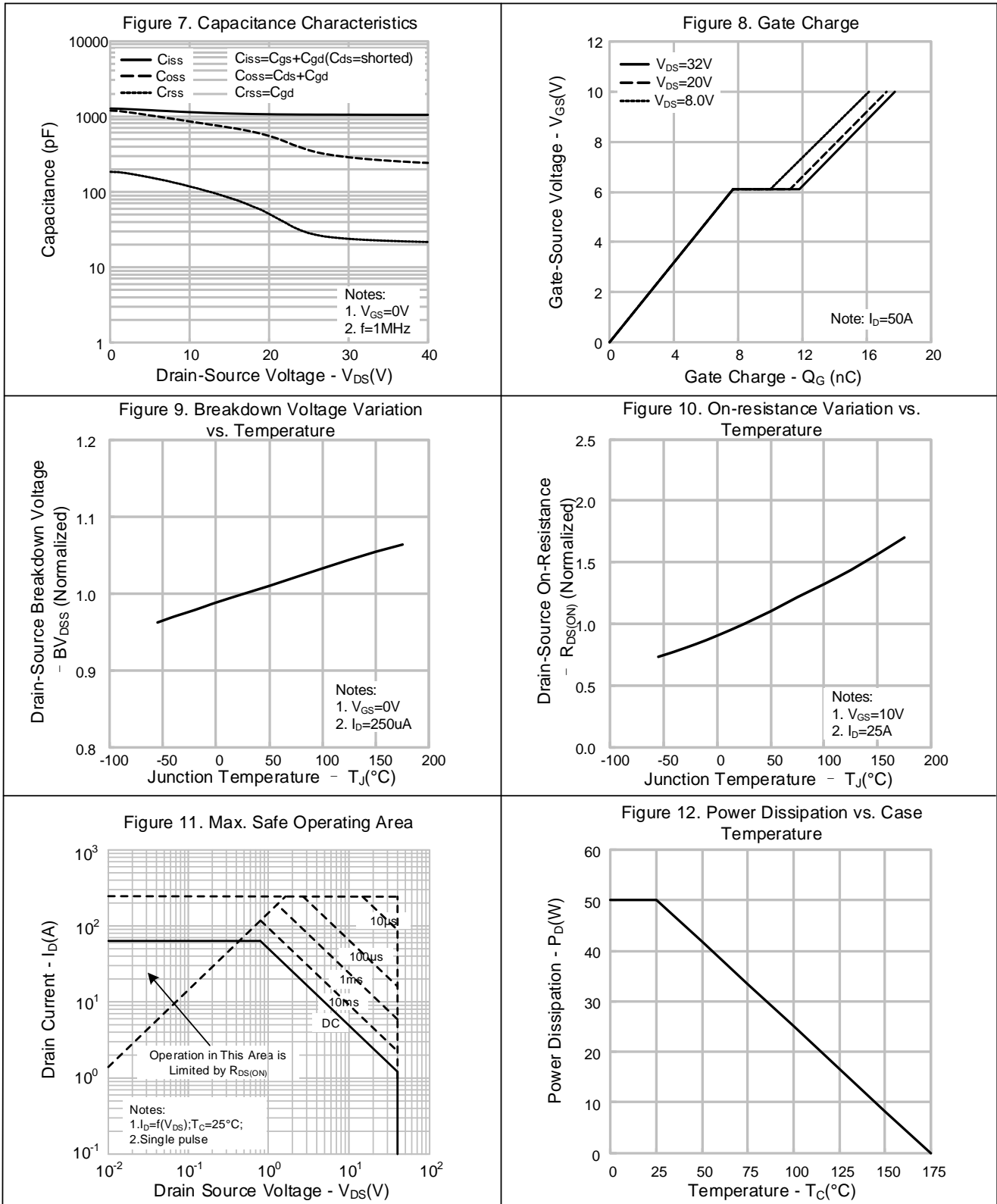
Notes:

- The rated value only refers to the maximum absolute value at the case temperature of 25°C in the specification. If the case temperature is higher than 25°C , it should be derated according to the actual environmental conditions;
- Pulse time $5\mu s$;
- The dissipation power will change with temperature, derating above 25°C : $0.33W/^{\circ}\text{C}$;
- Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
- Essentially independent of operating temperature.

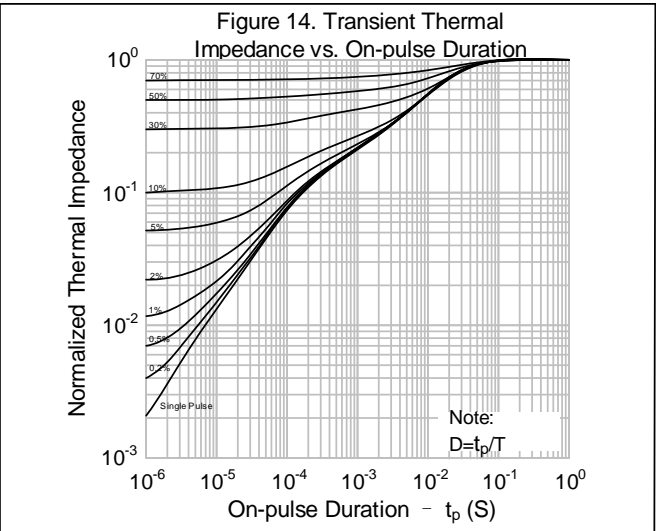
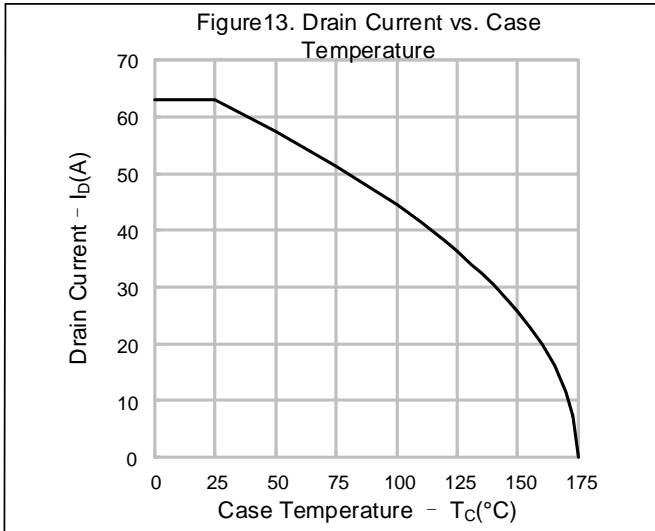
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (CONTINUED)

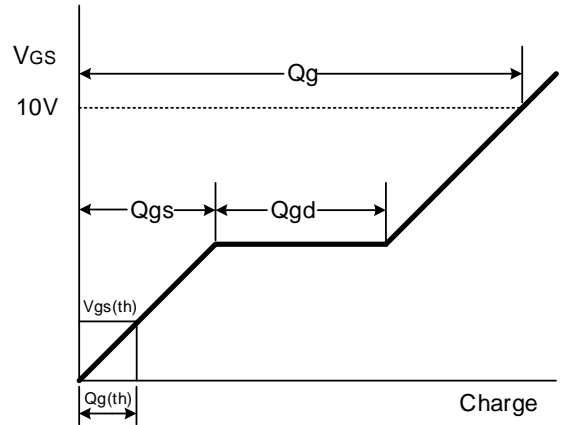
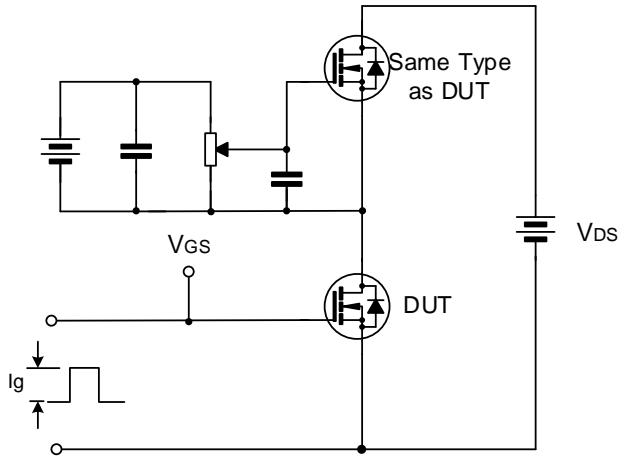


TYPICAL CHARACTERISTICS (CONTINUED)

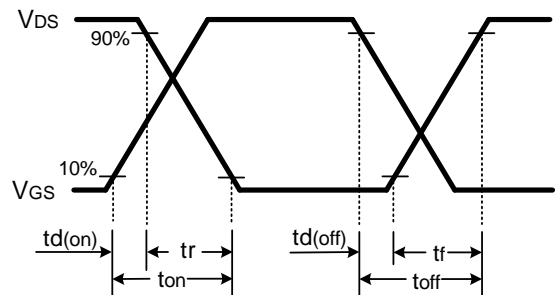
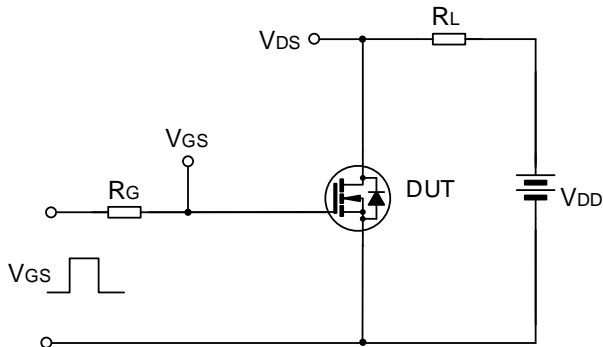


TYPICAL TEST CIRCUIT

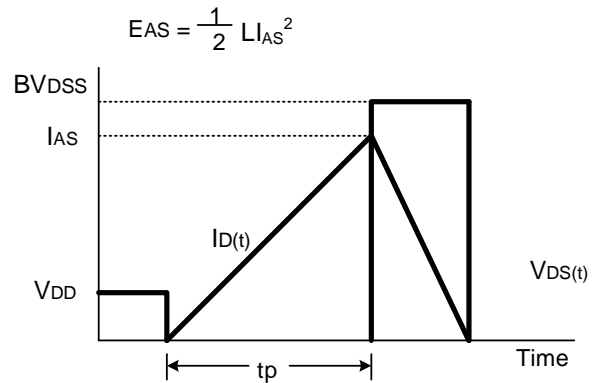
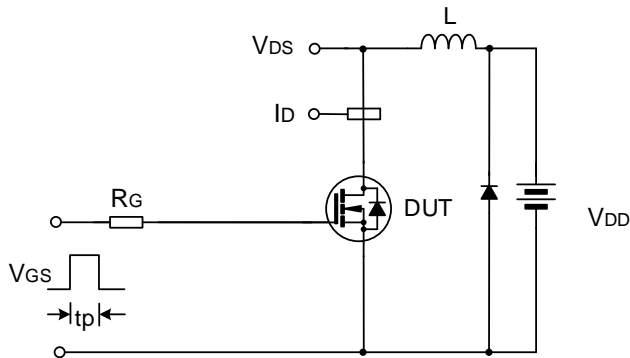
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



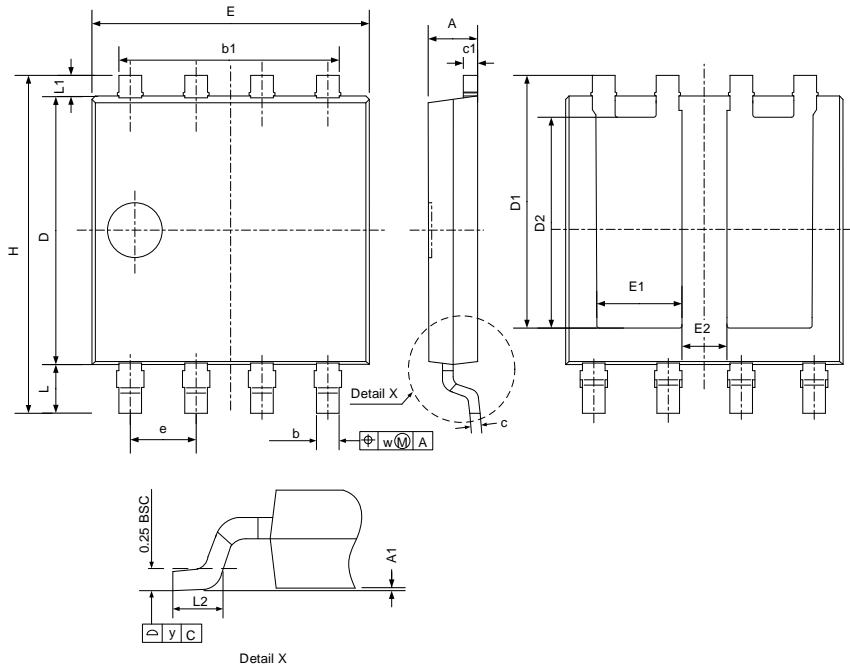
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

MO-4A-235-1.27

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.95	1.03	1.10
A1	0	0.05	0.10
b	0.35	0.42	0.50
b1	4.10	4.21	4.40
c	0.19	0.22	0.25
c1	0.24	0.27	0.30
D	4.45	4.59	4.70
D1	—	—	4.80
D2	3.50 REF		
E	4.95	5.10	5.30
E1	1.60	—	1.80
E2	—	—	0.85
e	1.27 BSC		
H	5.90	6.10	6.20
L	0.80	1.08	1.30
L1	0.30	0.44	0.55
L2	0.40	0.60	0.85
w	0.25		
y	0.10		



MOS DEVICES OPERATE NOTES:

Electrostatic charges may exist in many things. Please take following preventive measures to prevent effectively the MOS electric circuit as a result of the damage which is caused by discharge:

- The operator must put on wrist strap which should be earthed to against electrostatic.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed in antistatic/conductive containers for transportation.

Important notice :

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Rev.: **1.1**

Revision History:

1. Update features
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Rev.: **1.0**

Revision History:

1. First release
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