

100A, 30V N-CHANNEL MOSFET

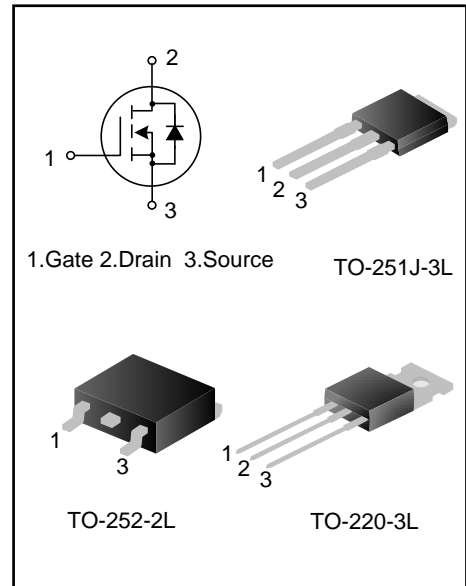
DESCRIPTION

The SVT035R5ND(MJ)(T) is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan's LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

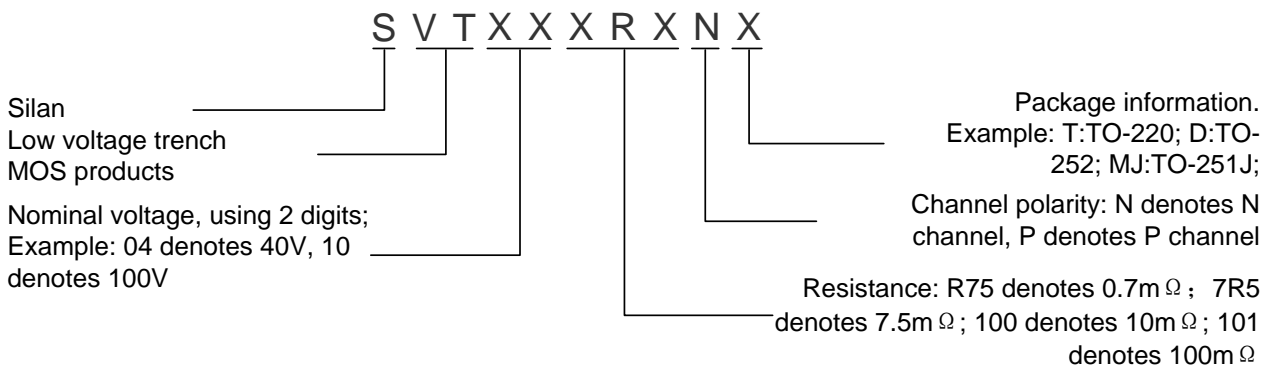
This device is widely used in the fields of uninterruptible power supplies and power management of inverter systems.

FEATURES

- ◆ 100A, 30V, $R_{DS(on)(typ.)}=4.0m\Omega @ V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low C_{rss}
- ◆ Fast switching
- ◆ Improved dv/dt capability



NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVT035R5NDTR	TO-252-2L	035R5ND	Halogen free	Tape&Reel
SVT035R5NMJ	TO-251J-3L	035R5NMJ	Halogen free	Tape
SVT035R5NT	TO-220-3L	035R5NT	Pb free	Tape

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, T_C=25°C)

Characteristics	Symbol	Ratings		Unit
		SVT035R5ND/MJ	SVT035R5NT	
Drain-Source Voltage	V _{DS}	30		V
Gate-Source Voltage	V _{GS}	±20		V
Drain Current	I _D	T _C =25°C		A
		T _C =100°C		
Drain Current Pulsed	I _{DM}	400		A
Power Dissipation (T _C =25°C) -Derate above 25°C	P _D	83	104	W
		0.7	0.8	W/°C
Single Pulsed Avalanche Energy (Note 1)	E _{AS}	200		mJ
Operation Junction Temperature Range	T _J	-55~+150		°C
Storage Temperature Range	T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVT035R5ND/MJ	SVT035R5NT	
Thermal Resistance, Junction-to-Case	R _{θJC}	1.52	1.2	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62	62.5	°C/W

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^\circ\text{C}$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1	1.6	2.5	V
Static Drain- Source	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	--	4.0	5.5	$m\Omega$
On State Resistance		$V_{GS}=4.5V, I_D=15A$	--	5.2	7.2	$m\Omega$
Gate Resistance	R_G	$f=1\text{MHz}$	--	4.9	--	Ω
Input Capacitance	C_{iss}	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=25V$	--	2190	--	pF
Output Capacitance	C_{oss}		--	268	--	
Reverse Transfer Capacitance	C_{riss}		--	206	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=4.5V, R_G=1.8\Omega, I_D=60A$ (Notes 2,3)	--	12.	--	ns
Turn-on Rise Time	t_r		--	88	--	
Turn-off Delay Time	$t_{d(off)}$		--	140	--	
Turn-off Fall Time	t_f		--	83	--	
Total Gate Charge	Q_g	$V_{DD}=24V, V_{GS}=10V, I_D=30A$ (Notes 2,3)	--	47	--	nC
Gate-Source Charge	Q_{gs}		--	8.5	--	
Gate-Drain Charge	Q_{gd}		--	9.9	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	100	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	400	
Diode Forward Voltage	V_{SD}	$I_S=20A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=30A, V_{GS}=0V,$	--	16	--	ns
Reverse Recovery Charge	Q_{rr}	$dI/dt=100A/\mu s$ (Note 2)	--	6.9	--	μC

Notes:

1. $L=0.5\text{mH}, V_{DD}=15V, V_G=10V, R_G=25\Omega,$ starting $T_J=25^\circ\text{C}$;
2. Pulse Test: Pulse width $\leq 300\mu s,$ Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. Output Characteristics

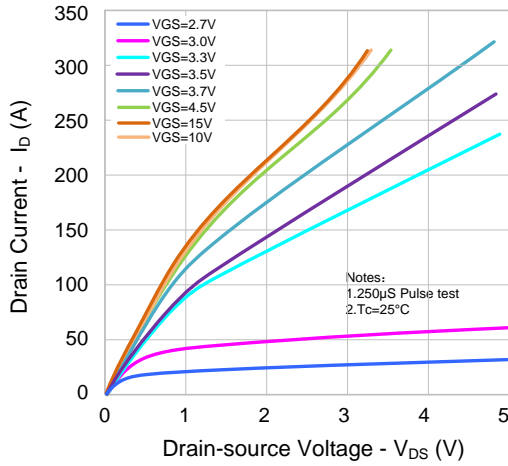


Figure 2. Transfer Characteristics

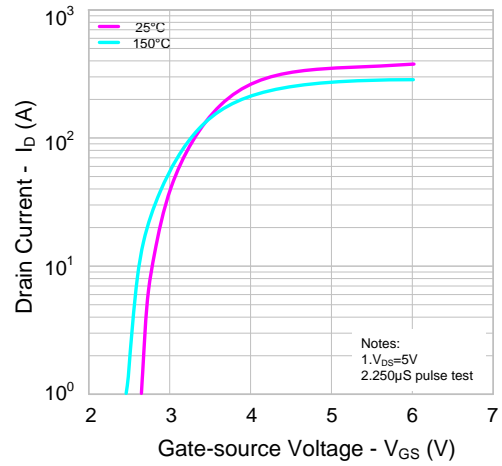


Figure 3. On-Resistance vs. Drain Current

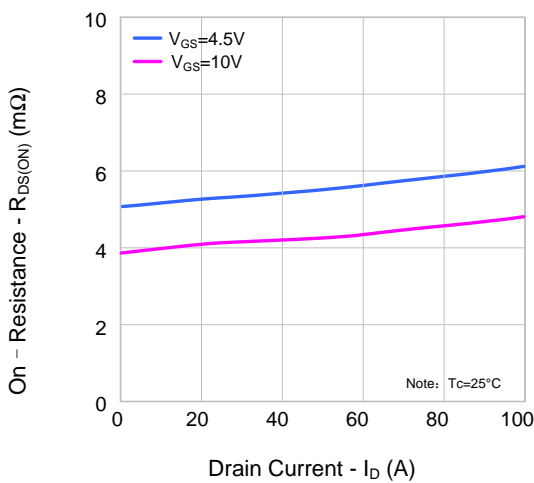


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

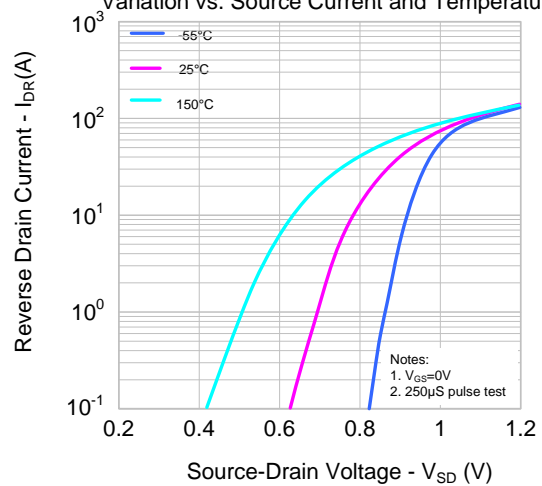


Figure 5. Capacitance Characteristics

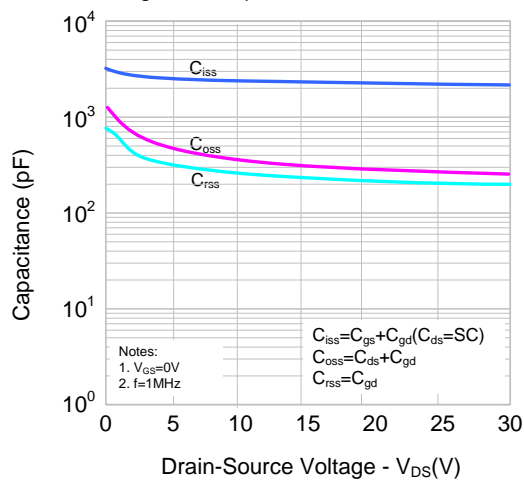
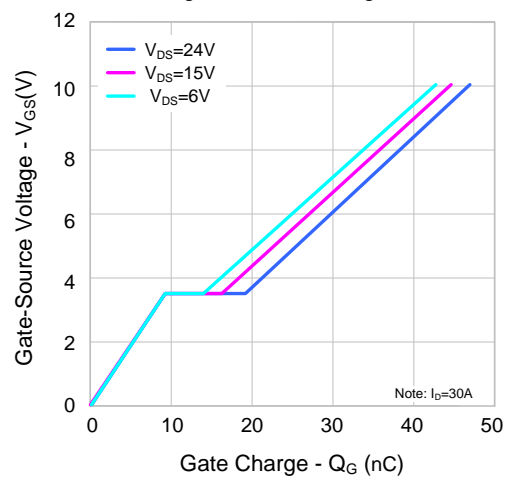
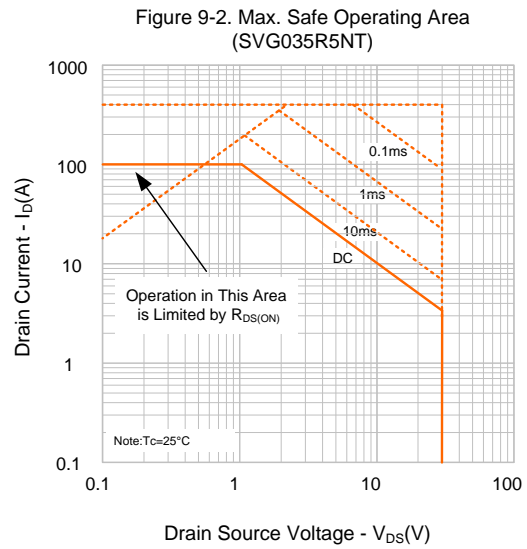
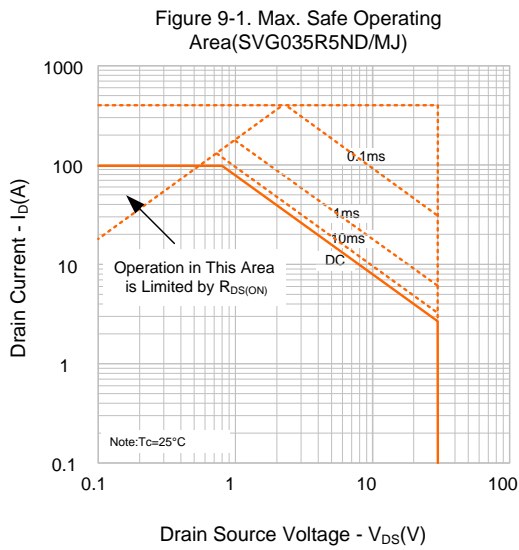
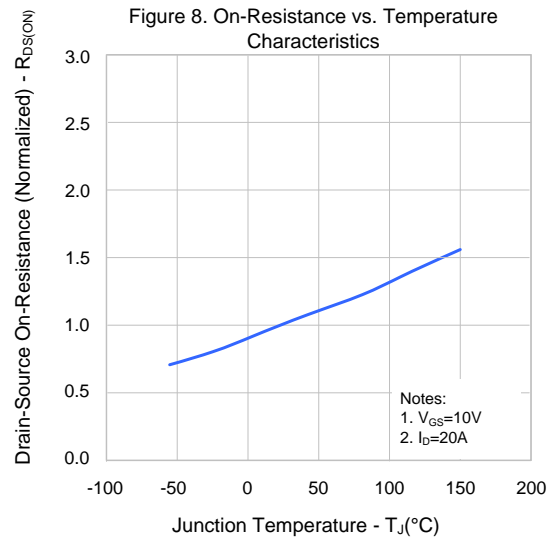
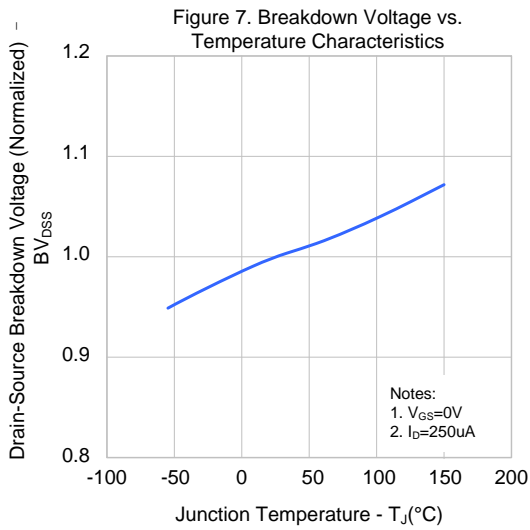


Figure 6. Gate Charge

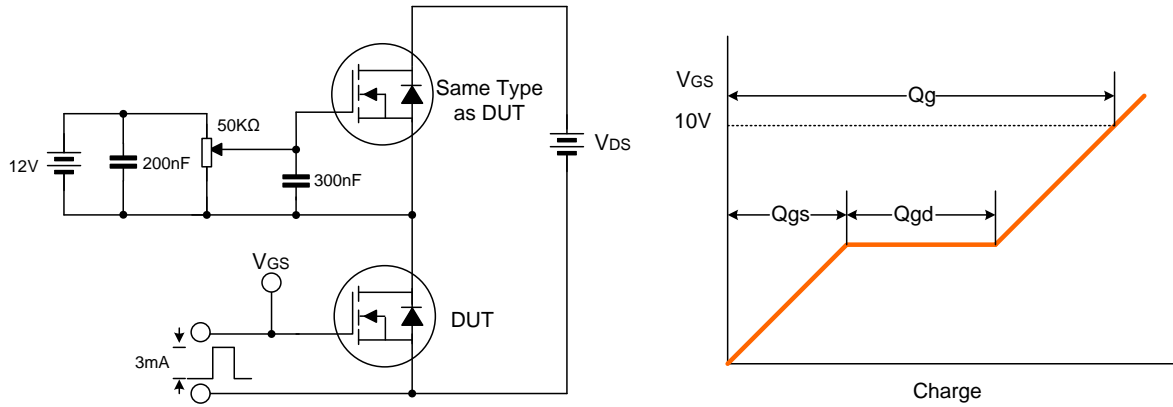


TYPICAL CHARACTERISTICS (continued)

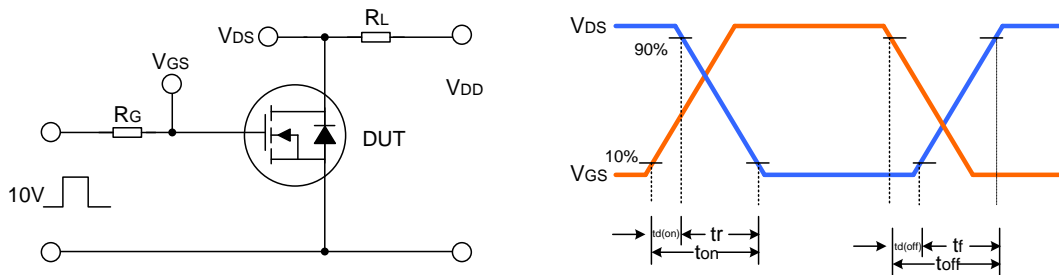


TYPICAL TEST CIRCUIT

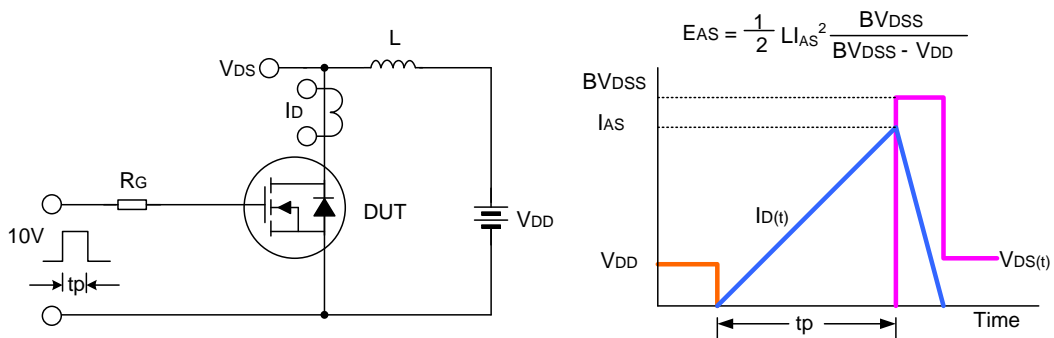
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



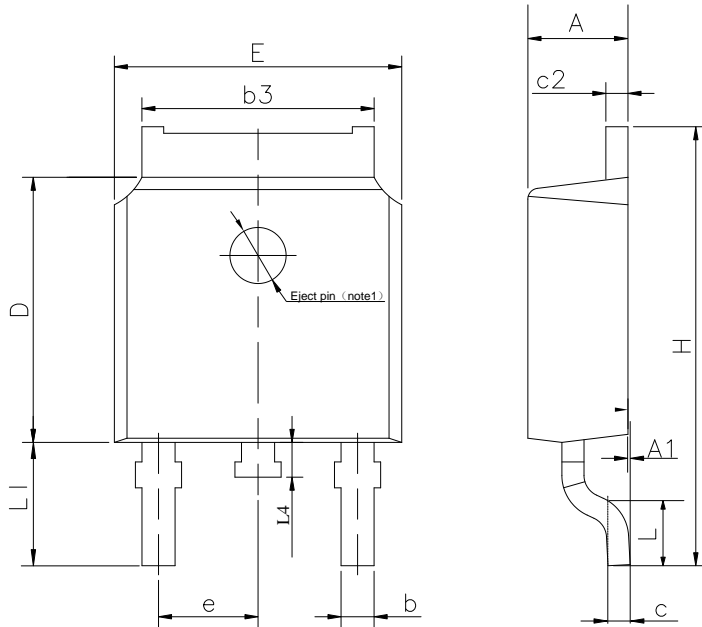
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

UNIT: mm

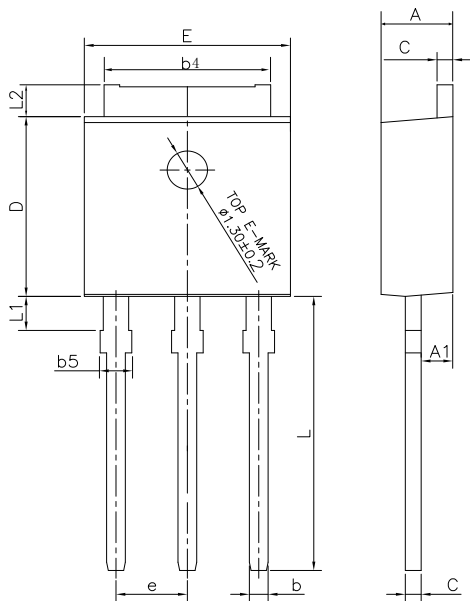


SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-251J-3L

UNIT: mm

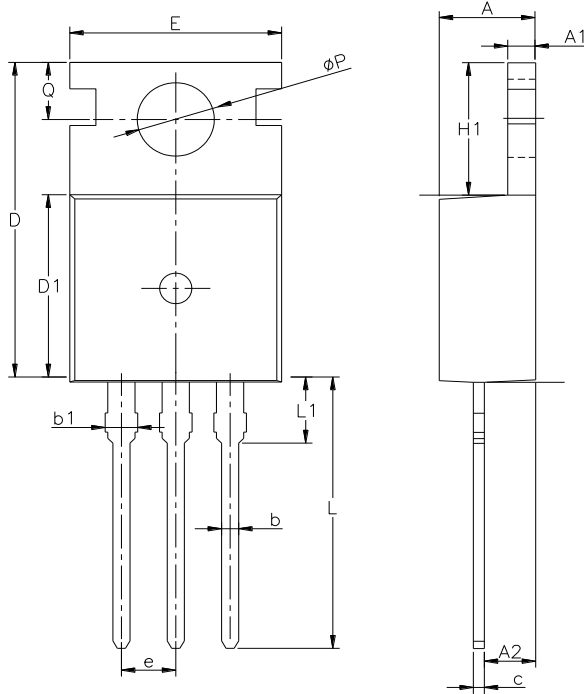


SYMBOL	MIN	NOM	MAX
A	2.18	2.30	2.39
A1	0.89	1.00	1.14
b	0.56	---	0.89
b4	4.95	5.33	5.46
b5	---	---	1.05
c	0.46	---	0.61
D	5.97	6.10	6.27
E	6.35	6.60	6.73
e	2.29 BCS		
L	8.89	9.30	9.65
L1	0.95	---	1.50
L2	0.89	---	1.27

PACKAGE OUTLINE

TO-220-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

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Rev: 1.1

Revision History:

1. Add SVT035R5NMJ(TO-251J-3L and SVT035R5NT(TO-220-3L)
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Rev: 1.0

Revision History:

1. First release
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